CLAIMS

1. A method of manufacturing a trench-gate semiconductor device comprising a semiconductor body having a plurality of transistor cells, each transistor cell being surrounded by a trench-gate comprising a trench extending into the semiconductor body with gate material in the trench, and each transistor cell having source and drain regions which are separated by a channel-accommodating region adjacent to the trench-gate, wherein the method includes the steps of:

(a) forming at a surface of the semiconductor body a first mask of a first material having first windows, each first window having a mid-point path coincident with a mid-point path of a said trench which will be formed later;

(b) forming on the semiconductor body a second mask having second windows, each second window being formed within and smaller than a said first window by providing two sidewall extensions to the first mask in the first window; and

(c) forming said trenches by etching into the semiconductor body at the second windows;

the method being characterised by the steps of:

(d) providing in each first window a continuous layer of a second material from which the second mask will be formed, the layer of second material having upright portions on the sidewalls of the first mask and a base portion on the surface of the semiconductor body;

(e) forming an intermediate mask of a third material in each first window covering the upright portions of the layer of second material and covering the base portion of the layer of second material except where the second window will be formed;

(f) using the intermediate mask in each first window to etch the base portion of said layer of second material and form said second window; and

(g) removing the intermediate mask to leave a pair of L-shaped parts of said second material within each first window as said two sidewall extensions to the first mask, each L-shaped part having a rectangular section base portion with a top surface parallel to the semiconductor body surface and a side surface perpendicular to the semiconductor body surface, and then carrying out step (c) to form said trenches.

2. A method as claimed in claim 1, wherein in step (d) the continuous layer of second material is also provided on top of the first mask, wherein in step (e) the third material is first deposited on the layer of second material on top of the first mask and in the first windows, and then the deposited third material is etched back to expose the layer of second material on top of the first mask and to leave the intermediate mask as two curved sidewall parts in each first window, and wherein in step (f) the layer of second material is also removed from the top of the first mask.

3. A method as claimed in claim 1 or claim 2, wherein the method further includes providing an insulating layer in each trench, depositing said gate material in each trench on said insulating layer to form a gate for each trench-gate, and providing a gate insulating overlayer over each said gate.

4. A method as claimed in any one of claims 1 to 3, wherein the semiconductor body is monocrystalline silicon, the first material is silicon dioxide, and the second material is silicon nitride.

5. A method as claimed in any one of claims 1 to 4, wherein the method includes the further steps of:

(h) providing a fourth material between the L-shaped parts within each said first window to the top of the first window; and

(i) removing the first mask to expose the semiconductor body

surface between each pair of L-shaped parts.

6. A method as claimed in any one of claims 1 to 5, wherein the semiconductor device is a vertical power transistor and wherein each transistor cell has an annular source region adjacent to a top part of the trench-gate.

7. A method as claimed in claim 6 as dependent on claim 5, wherein regions of conductivity type suitable for the annular source regions are formed in an upper part of the semiconductor body by dopant implantation through said first windows before step (d), wherein forming the trenches in step (c) removes central portions of the implanted regions to provide the annular source regions, and wherein a source electrode is provided after step (i), the source electrode extending over the L-shaped parts and over the fourth material between the L-shaped parts, and the source electrode contacting the annular source regions and the semiconductor body surface within and adjacent the source regions.

8. A method as claimed in claim 6 as dependent on claim 5, wherein the semiconductor body is provided with an upper layer of conductivity type suitable for the annular source regions before forming the first mask in step (a), wherein said upper layer of the semiconductor body is etched after step (i) using the L-shaped parts and the fourth material as an etchant mask to provide the annular source regions having a lateral extent defined by the L-shaped parts, and wherein after providing the annular source regions a source electrode is provided, the source electrode extending over the L-shaped parts and over the fourth material between the L-shaped parts, and the source electrode contacting the annular source regions and the semiconductor body surface within and adjacent the source regions.

9. A method as claimed in claim 6 as dependent on claim 5, wherein spacers are formed after step (i) with each spacer having a vertical surface aligned with an outer surface of a said upright portion of second material and a horizontal base surface on the semiconductor body surface, wherein the spacers are used to form the annular source regions with the lateral extent of the source regions from the trench-gates being determined by the lateral extent of the base surface of the spacers, and wherein a source electrode is provided to contact the annular source regions and the semiconductor body surface within and adjacent to the source regions.

10. A method as claimed in claim 9, wherein regions of one conductivity type suitable for the annular source regions are present in upper parts of the semiconductor body and exposed between each pair of L-shaped parts after step (i) and before forming the spacers, and wherein the annular source regions are formed by etching the regions of one conductivity using the spacers as a mask.

11. A method as claimed in claim 10, wherein said etching to form the source regions exposes side surfaces of the source regions, and wherein the spacers are then etched to expose top surfaces of the source regions, whereby the source electrode contacts the source region side surfaces and the source region exposed top surfaces.

12. A method as claimed in claim 10 or claim 11, wherein the regions of one conductivity type are formed by dopant implantation and diffusion after removing the first mask.

13. A method as claimed in any one of claims 10 to 12, wherein a gate insulating overlayer is provided over the gate material of each trench-gate before providing the fourth material between the L-shaped parts in step

(h), and wherein said fourth material is present when said spacers are formed and when the annular source regions are formed by etching.

14. A method as claimed in any one of claims 10 to 12, wherein the fourth material between the L-shaped parts is removed after step (i) and before forming the spacers, wherein the spacers are of insulating material, and wherein, at the same time as the spacers are formed with each said spacer vertical surface aligned with an outer surface of a said upright portion of second material, further spacers are formed against inner surfaces of the upright portions and these further spacers merge to provide a gate insulating overlayer.

15. A method as claimed in any one of claims 1 to 5, wherein the semiconductor device is a memory device having a plurality of memory cells, each memory cell comprising a said transistor cell as a switching transistor and comprising a trench storage capacitor, wherein the method includes providing a capacitor electrode for a said storage capacitor in a lower portion of each trench, providing a capacitor insulating layer in each trench over said capacitor electrode, and providing said gate material for a said switching transistor trench-gate in an upper portion of each trench above the capacitor insulating layer.

16. A trench-gate power transistor manufactured by the method as claimed in any one of claims 6 to 14.

17. A power transistor as claimed in claim 16, wherein the transistor cells have a pitch in the range 1μm to 3μm, the trenches have a width in the range 0.1μm to 0.4μm, and the trenches have a depth in the range 0.5μm to 3μm.

18. A power transistor as claimed in claim 16 or claim 17, wherein the transistor cells are adapted to withstand a specified source-drain voltage in the off-condition, the specified voltage being in the range up to about 50 volts.

19. A power transistor as claimed in claim 18, wherein the transistor cells are configured in a two-dimensionally repetitive pattern.

20. A memory device manufactured by the method as claimed in claim 15.